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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,524	06/23/2003	Ming-Dou Ker	0941-0759P	8633
2292 7590 12/19/2006 BIRCH STEWART KOLASCH & BIRCH PO BOX 747			EXAMINER	
			LIU, BENJAMIN T	
FALLS CHUR	CH, VA 22040-0747		ART UNIT	PAPER NUMBER
			2826	
			-	
SHORTENED STATUTOR	Y PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE	
3 MONTHS		12/19/2006	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)				
* * *	10/600,524	KER ET AL.				
Office Action Summary						
<i></i>	Examiner	Art Unit				
The MAILING DATE of this communication and	Benjamin T. Liu	2826				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA.  - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period variety of the second of th	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim vill apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	i. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 28 A	<u>ugust 2006</u> .					
2a) ☐ This action is <b>FINAL</b> . 2b) ☑ This	<u>_</u>					
3) Since this application is in condition for allowar	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-10</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-10</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/o	r election requirement.	•				
Application Papers						
9) The specification is objected to by the Examine	ar					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)⊡ Some * c)⊡ None of:						
<ol> <li>Certified copies of the priority documents have been received.</li> </ol>						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
Notice of References Cited (PTO-892)     Notice of Draftsperson's Patent Drawing Review (PTO-948)	4)					
3) Information Disclosure Statement(s) (PTO/SB/08)  5) Notice of Informal Patent Application						
Paper No(s)/Mail Date 6)  Other:						

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#### **DETAILED ACTION**

1. Claims 11-104 cancelled in 8/28/06.

#### Oath/Declaration

2. The oath/declaration filed on 6/23/03 is acceptable.

## **Drawings**

3. The formal drawings filed on 6/23/03 are acceptable.

### **Priority**

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### Information Disclosure Statement

5. Applicants have not submitted an Information Disclosure Statement.

## Allowable Subject Matter

6. The indicated allowability of claims 1-10 are withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

## Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C 103(a) as being unpatentable over Lin (2002/0175377) in view of Cai (6,830,966).

With regard to claim 1, figures 2 and 3B of Lin discloses an ESD protection device comprising: a substrate 30; an isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin) on the substrate 30, enclosing an active region 14; a first gate (12 top of fig. 2 of Lin) having two ends (12 top left and right of fig. 2 of Lin) overlapping the isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin) to stretch over the active region 14, and coupled to a first node Gate; a second gate (20c top left of fig. 2 of Lin) disposed on a first side 14b of the first gate (12 top of fig. 2 of Lin) and near the first end (12 top left of fig. 2 of Lin) of the first gate (12 top of fig. 2 of Lin); a first 22 and second doping 14a regions at the first 14b and second 14a sides of the first gate (12 top of fig. 2 of Lin), and the first doping region 22 and first side 14b of the first gate (12 top of fig. 2 of Lin) coupled to a second node Anode, wherein the first doping region 22 has a first discontinuity region (under 20c top left of fig. 2 of Lin), without source 14a/drain 22 implantation in the substrate 30 under the second gate (20c top left of fig. 2 of Lin).

Lin does not disclose the second doping region and second side of the first gate coupled to a first node.

However, figure 1 of Cai et al. discloses the source 22 coupled to the gate 30.

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Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Lin with the limitation of Cai in order to provide a low resistance discharge path. (Note lines 2-3 paragraph [0006] of Cai)

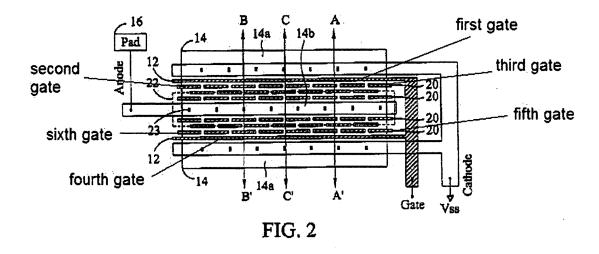


Figure 1: first, second, third, fourth, fifth, and sixth gates

With regard to claim 2, figures 2 and 3C of Lin discloses the limitation, wherein the isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin) is a shallow trench isolation.

With regard to claim 3, figures 2 and 3C of Lin discloses the limitation, wherein the first node Cathode is ground Vss while the second node Anode is a pad 16.

With regard to claim 4, figures 2 and 3C of Lin discloses a third gate (20c top right of fig. 2 of Lin) disposed at the first side 14b of the first gate (12 top of fig. 2 of Lin) and near the second end (12 top right of fig. 2 of Lin) of the first gate (12 top of fig. 2 of Lin), wherein the first doping region 22 has a second discontinuity region (under 20c top

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right of fig. 2 of Lin), without source 14a/drain 22 implantation, in the substrate 30 under the third gate (20c top right of fig. 2 of Lin).

With regard to claim 5, figures 2 and 3C of Lin discloses the limitation, wherein a fourth gate (12 bottom of fig. 2 of Lin) having a first and second end (12 bottom left and right of fig. 2 of Lin) overlapping the isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin) to stretch over the active region 14, and coupled to the first node Gate, wherein the first doping region 22 is between the first (12 top of fig. 2 of Lin) and fourth gate (12 bottom of fig. 2 of Lin); a fifth (20c bottom left of fig. 2 of Lin) and sixth gate (20c bottom right of fig. 2 of Lin) both disposed at a first side 14b of the fourth gate (20c bottom of fig. 2 of Lin), and respectively near a first and second end of the fourth gate (12 bottom left and right of fig. 2 of Lin), wherein the first doping region 22 has a third (under 20c bottom left of fig. 2 of Lin) and fourth (under 20c bottom right of fig. 2 of Lin) discontinuity region, without source 14a /drain 22 implantation, respectively in the substrate 30 under the fifth (20c bottom left of fig. 2 of Lin) and sixth gate (20c bottom right of fig. 2 of Lin); and

Lin does not disclose a third doping region on a second side of the fourth gate and coupled to the second node.

However, figure 1 of Cai et al. discloses the source 22 coupled to the gate 30.

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Lin with the limitation of Cai in order to provide a low resistance discharge path. (Note lines 2-3 paragraph [0006] of Cai)

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With regard to claim 6, figures 2 and 3C of Lin discloses the limitation, wherein each of the second, third, fifth and sixth gate (20c top left and right and bottom left and right of fig. 2 of Lin) has one end overlapping the isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin).

With regard to claim 7, figures 2 and 3C of Lin discloses the limitation, wherein each of the first, second, third, fourth, fifth and sixth gate (12 top, 20c top left and right, 12 bottom, and 20c bottom left and right of fig. 2 of Lin) comprises: a conducting layer ("poly gates 12" line 4 paragraph [0034] and "poly segments 36" line 1 paragraph [0035] of Lin); a gate oxide layer ("NMOS" line 4 paragraph [0034] and "gate oxide segments 38" line 1 paragraph [0035] of Lin) under the conducting layer ("poly gates 12" line 4 paragraph [0034] and "poly segments 36" line 1 paragraph [0035] of Lin); and a first and second spacer (spacers on 12 and 20c) respectively adjacent to two sides of the conducting layer ("poly gates 12" line 4 paragraph [0034] and "poly segments 36" line 1 paragraph [0035] of Lin) and gate oxide layer ("NMOS" line 4 paragraph [0034] and "gate oxide segments 38" line 1 paragraph [0035] of Lin).

With regard to claim 8, figures 2 and 3C of Lin discloses the limitation, wherein the conducting layer (12, 36) is a polysilicon layer ("poly gates 12" line 4 paragraph [0034] and "poly segments 36" line 1 paragraph [0035] of Lin) while the gate oxide layer ("NMOS" line 4 paragraph [0034] and "gate oxide segments 38" line 1 paragraph [0035] of Lin), and the first and second spacer (spacers of 12 and 20c).

Lin does not disclose the spacers are silicon oxide layers.

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However, figure 1 of Cai et al. discloses spacers 17 that are silicon oxide ("oxide spacers" line 10 paragraph [0026] of Cai et al.) layers.

Therefore, it would have been obvious to one of ordinary skill in the art to form the device of Lin with the limitation of Cai et al. in order to form the mask for implantation of the n+ source and drain regions. (Note line 13 paragraph [0026] of Cai et al.)

With regard to claim 9, figures 2 and 3C of Lin discloses the limitation, a fourth doping region ("p+ guard-ring region 32" line 8 paragraph [0036] of Lin) enclosing the isolation region ("shallow trench isolation (STI) region" lines 6-7 paragraph [0034] of Lin).

With regard to claim 10, figures 2 and 3C of Lin discloses the limitation, wherein the substrate 30 is a P substrate ("p-substrate" line 7 paragraph [0036] of Lin), the first 22, second (14a top of fig. 2 of Lin) and third (14a bottom of fig. 2 of Lin) doping region are N doping regions ("n-doped" line 9 paragraph [0034] of Lin), and the fourth doping region ("p+ guard-ring region 32" line 8 paragraph [0036] of Lin) is a P doping region.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 571 272 1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTL 12/12/2006

EONARDO ANDUJAR